

# Interconnect RC And Layout Extraction For VLSI

## By Qing K. Zhu

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Patents Publication number RC interconnect extraction 1228 extracts layout parasitics for selected nets or RC interconnect extraction 1228 creates an R and C

<http://www.google.com/patents/US6438729>

and Y. Zheng, "Compression Algorithms for Dummy Fill VLSI Layout B. Yao and Z. Zhu K. Samadi and P. Sharma, "Interconnect Modeling for Improved

<http://vlsicad.ucsd.edu/Publications/Conferences/>

A reliable quick parasitic capacitance extraction tool for the physical layer in communication (VLSI) form the basis for Zhu QK (2002) Interconnect RC and

<http://link.springer.com/article/10.1007%2Fs12652-009-0002-6>

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In electronic design automation, parasitic extraction is calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an

[http://en.wikipedia.org/wiki/Parasitic\\_extraction](http://en.wikipedia.org/wiki/Parasitic_extraction)

Publications; Software Releases N. Hasan, J. Cong, P. Mckinley and C. L. Liu. Fault Covering Problems in Reconfigurable VLSI J. Cong, J. Shinnerl, K. Sze

<http://cadlab.cs.ucla.edu/beta/cadlab/publications>

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<http://www.bokus.com/bok/9781441953360/high-speed-clock-network-design/>

Calculating frequency-dependent inductance of VLSI interconnect by complete multiple reciprocity extraction. Several approaches a VLSI layout is considered

<http://dl.acm.org/citation.cfm?id=1118299.1118491>

IEEE Transactions on Very Large Scale Integration Inhee Lee, Qing Manycore Interconnect Fabric," IEEE Symposium on VLSI

<http://blaauw.eecs.umich.edu/resource.php?grp=1>

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BEOL Variability and Impact on RC Extraction Nagaraj NS, Design, Performance, process realities and interconnect extraction [1].

[http://videos.dac.com/42nd/papers/46\\_1.pdf](http://videos.dac.com/42nd/papers/46_1.pdf)

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2007 IC/CAD Contest Problem B3 Interconnect Parasitic RC Extraction Source: Cadence Design Systems, Inc. 1. Introduction In submicron processes, signal delay due

[http://www.ee.ncu.edu.tw/~cad\\_contest/Problems/95/PB3/2007\\_B3.pdf](http://www.ee.ncu.edu.tw/~cad_contest/Problems/95/PB3/2007_B3.pdf)

Extracting simple but accurate RC models for VLSI interconnect. From a background of RC interconnect models in layout-to and layout extraction for

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IC package interconnect modeling; and general pre-layout software tool used for layout-to-circuit device and interconnect RC extraction of

<http://www.optem.com/submicron-ic.php>

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by Qing Zhu, Wayne W.M. Dai, Joe G. Xi The clock network can exhibit distributed RC and lossy Our models comprehend key interconnect circuit and layout

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when compared to traditional layout extraction (2D PARASITIC EXTRACTION Interconnect capacitance in each node in a model for RC extraction, e.g, distributed

<http://www2.computer.org/portal/web/csdl/doi/10.1109/SBCCI.2000.876050>

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Postlayout EDA tools lock onto and a final performance simulation that uses interconnect RC Simon, "Technical White Paper on RC Extraction," Epic Design

<http://www.edn.com/electronics-products/other/4348742/Postlayout-EDA-tools-lock-onto-full-chip-verification>

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of the IFIP/IEEE International Conference on Very Large Scale Integration Q. Zhu, K . Vaidyanathan, O L. Pileggi, RC(L)Interconnect Sizing With Second

<http://users.ece.cmu.edu/~pileggi/publications/refereed-conference-publications/>

State of the art in interconnect extraction is mostly RC. Post layout extraction for high frequency design On chip Interconnect Design of critical wires

[http://www.research.ibm.com/haifa/Workshops/summerseminar2004/present/summer\\_phd\\_seminar04.pdf](http://www.research.ibm.com/haifa/Workshops/summerseminar2004/present/summer_phd_seminar04.pdf)

View Tony Nguyen's professional profile on LinkedIn. Strong background in custom IC Layout. Qing Zhu. Hoa Ngo. Sr. CAD Engineer at RFMD.

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The HDR Book: Unlocking the Pros Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits By Wenjian Yu, Interconnect RC and Layout

<http://avxsearch.se/?q=RC%20BOOK>

interconnect RC is a significant portion of circuit performance, In a typical design flow, parasitic extraction and timing analysis are two independent steps.

<http://doi.ieeecomputersociety.org/10.1109/VLSID.2006.148>

Qing K. Zhu and Paige Kolze MOS Layout CHES: A Comprehensive Tool for CDFG Extraction and Synthesis

<http://www.computer.org/csdl/proceedings/isvlsi/2006/2533/00/01602405.pdf>