Interconnect RC And Layout Extraction For VLSI By Qing K. Zhu

By Qing K. Zhu

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Calculating frequency-dependent inductance of VLSI interconnect by complete multiple reciprocity extraction. Several approaches a VLSI layout is considered
http://dl.acm.org/citation.cfm?id=1118299.1118491

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Hi, I am trying to do top level interconnect extraction using Calibre RCX. This is a mixed signal design (most sub-blocks using analog flow + one digital block which
https://communities.mentor.com/thread/3133

Qing K. Zhu and Paige Kolze MOS Layout CHESS: A Comprehensive Tool for CDFG Extraction and Synthesis
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when compared to traditional layout extraction (2D PARASITIC EXTRACTION Interconnect capacitance in each node in a model for RC extraction, e.g, distributed
http://www2.computer.org/portal/web/csdl/doi/10.1109/SBCCI.2000.876050

View Tony Nguyen's professional profile on LinkedIn. Strong background in custom IC Layout. Qing Zhu. Hoa Ngo. Sr. CAD Engineer at RFMD.
https://www.linkedin.com/pub/tony-nguyen/5/6B3/2B5

We focus on interconnect design, extraction, and 2D/3D substrate and interconnect RC extraction for detailed analysis of crosstalk and delay effects at the cell
http://s23.a2zinc.net/clients/MPAssociates/52DAC/Public/eBooth.aspx?FromPage=Exhibitors.aspx&ParentBoothID=&ListByBooth=true&BoothID=105458

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interconnect and substrate extraction software tool for techniques are used to accurately and efficiently extract these RC values from the layout.
http://www.optem.com/inspector.php
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A reliable quick parasitic capacitance extraction tool for the physical layer in communication (VLSI) form the basis for Zhu QK (2002) Interconnect RC and
http://link.springer.com/article/10.1007%2Fs12652-009-0002-6

and Y. Zheng, "Compression Algorithms for Dummy Fill VLSI Layout B. Yao and Z. Zhu K. Samadi and P. Sharma, "Interconnect Modeling for Improved
http://vlsicad.ucsd.edu/Publications/Conferences/

2007 IC/CAD Contest Problem B3 Interconnect Parasitic RC Extraction Source: Cadence Design Systems, Inc. 1. Introduction In submicron processes, signal delay due
http://www.ee.ncu.edu.tw/~cad_contest/Problems/95/PB3/2007_B3.pdf

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Patents Publication number RC interconnect extraction 1228 extracts layout parasitics for selected nets or RC interconnect extraction 1228 creates an R and C
http://www.google.com/patents/US6438729

State of the art in interconnect extraction is mostly RC. Post layout extraction for high frequency design On chip Interconnect Design of critical wires
http://www.research.ibm.com/haifa/Workshops/summerseminar2004/present/summer_phd_seminar04.pdf

This paper presents an efficient algorithm for buffered Steiner tree construction with "Interconnect Layout extraction of interconnect parasitics in VLSI
http://dl.acm.org/citation.cfm?id=244522.244530&coll=DL&dl=ACM