

Interconnect RC And Layout Extraction For VLSI

By Qing K. Zhu

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Accelerate Design Closure. in-design, pre-LVS and post-extraction parasitic analysis. Handles large RC networks like power mesh; Interconnect calculator for
<http://www.icscape.com/index.php/products/by-function/interconnect-analysis>

Extracting simple but accurate RC models for VLSI interconnect. From a background of RC interconnect models in layout-to and layout extraction for

<http://citeseerx.ist.psu.edu/showciting?cid=842355>

LASCA-interconnect parasitic extraction tool for deep-submicron IC design Full Text Sign RC models; VLSI; layout extraction; polygon distribution;

http://ieeexplore.ieee.org/xpl/abstractKeywords.jsp?reload=true&arnumber=876050&sortType%3Dasc_p_Sequence%26filter%3DAND%28p_IS_Number%3A18940%29

Hi, I am trying to do top level interconnect extraction using Calibre RCX. This is a mixed signal design (most sub-blocks using analog flow + one digital block which

<https://communities.mentor.com/thread/3133>

Browse Journals & Magazines > Very Large Scale Integration Zhu, Qing K . (1 interconnect lines by partitioning the RC interconnect lines with <http://ieeexplore.ieee.org/xpl/tocresult.jsp?reload=true&isnumber=10826>

This paper presents an efficient algorithm for buffered Steiner tree construction with "Interconnect Layout extraction of interconnect parasitics in VLSI

<http://dl.acm.org/citation.cfm?id=244522.244530&coll=DL&dl=ACM>

BEOL Variability and Impact on RC Extraction Nagaraj NS, Design, Performance, process realities and interconnect extraction [1].

http://videos.dac.com/42nd/papers/46_1.pdf

interconnect and substrate extraction software tool for techniques are used to accurately and efficiently extract these RC values from the layout.

<http://www.optem.com/inspector.php>

High-Speed Clock Network Design has 2 available editions to buy at Alibris. " by Qing K. Zhu. Interconnect Rc and Layout Extraction for VLSI

<http://www.alibris.com/High-Speed-Clock-Network-Design-Qing-K-Zhu/book/7622052>

Qing K. Zhu and Paige Kolze MOS Layout CHES: A Comprehensive Tool for CDFG Extraction and Synthesis

<http://www.computer.org/csdl/proceedings/isvlsi/2006/2533/00/01602405.pdf>

We focus on interconnect design, extraction, and 2D/3D substrate and interconnect RC extraction for detailed analysis of crosstalk and delay effects at the cell

<http://s23.a2zinc.net/clients/MPAssociates/52DAC/Public/eBooth.aspx?FromPage=Exhibitors.aspx&ParentBoothID=&ListByBooth=true&BoothID=105458>

Qing K. Zhu is the author Power Distribution Network Design for VLSI 3.5 of 5 stars 3.50 avg Interconnect Rc and Layout Extraction for VLSI 0.0 of 5 stars 0

http://www.goodreads.com/author/show/882204.Qing_K_Zhu

of the IFIP/IEEE International Conference on Very Large Scale Integration Q. Zhu, K . Vaidyanathan, O L. Pileggi, RC(L)Interconnect Sizing With Second

<http://users.ece.cmu.edu/~pileggi/publications/refereed-conference-publications/>

Optimization with Recourse of Analog Circuits including Layout Extraction, Capacitance of RC Interconnect, for VLSI Interconnect
<http://users.ece.cmu.edu/~pileggi/publications/publications/>

High-Speed Clock Network Design is a collection of design Power Distribution Network Design for VLSI Qing K Zhu Inbunden Layout guidelines. 5
<http://www.bokus.com/bok/9781441953360/high-speed-clock-network-design/>

Postlayout EDA tools lock onto and a final performance simulation that uses interconnect RC Simon, "Technical White Paper on RC Extraction," Epic Design
<http://www.edn.com/electronics-products/other/4348742/Postlayout-EDA-tools-lock-onto-full-chip-verification>

Qing K. Zhu, "Interconnect RC and Layout Extraction for VLSI" Trafford Publishing | 2002 | ISBN: 155395369X | 150 pages | Djvu | 1,4 MB
<http://avxsearch.se/?q=CADS%20RC>

der Meijs, "Extracting Simple but Accurate RC Models for VLSI Interconnect. and layout extraction for interconnect resistance extraction by
<http://citeseerx.ist.psu.edu/showciting?cid=2392566>

State of the art in interconnect extraction is mostly RC. Post layout extraction for high frequency design On chip Interconnect Design of critical wires
http://www.research.ibm.com/haifa/Workshops/summerseminar2004/present/summer_phd_seminar04.pdf

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<http://en.bookfi.org/g/Qing%20K.%20Zhu>

IEEE Transactions on Very Large Scale Integration Inhee Lee, Qing Manycore Interconnect Fabric," IEEE Symposium on VLSI
<http://blaauw.eecs.umich.edu/resource.php?grp=1>

Performance optimization of VLSI interconnect layout. Jason survey of existing techniques for interconnect optimization during the VLSI physical
<http://www.sciencedirect.com/science/article/pii/S0167926096000089>

The HDR Book: Unlocking the Pros Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits By Wenjian Yu, Interconnect RC and Layout

<http://avxsearch.se/?q=RC%20BOOK>

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A reliable quick parasitic capacitance extraction tool for the physical layer in communication (VLSI) form the basis for Zhu QK (2002) Interconnect RC and

<http://link.springer.com/article/10.1007%2Fs12652-009-0002-6>

In electronic design automation, parasitic extraction is calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an

http://en.wikipedia.org/wiki/Parasitic_extraction

Inductance calculations, working formulas and extraction, substrate, VLSI interconnect. demonstrated by extraction from a real layout design that

<http://citeseerx.ist.psu.edu/showciting?cid=211641>

and Y. Zheng, "Compression Algorithms for Dummy Fill VLSI Layout B. Yao and Z. Zhu K. Samadi and P. Sharma, "Interconnect Modeling for Improved

<http://vlsicad.ucsd.edu/Publications/Conferences/>