Interconnect RC And Layout Extraction For VLSI By Qing K. Zhu

By Qing K. Zhu

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A reliable quick parasitic capacitance extraction tool for the physical layer in communication (VLSI) form the basis for Zhu QK (2002) Interconnect RC and
http://link.springer.com/article/10.1007%2Fs12652-009-0002-6

IC package interconnect modeling; and general pre-layout software tool used for layout-to-circuit device and interconnect RC extraction of
http://www.optem.com/submicron-ic.php

Patents Publication number RC interconnect extraction 1228 extracts layout parasitics for selected nets or RC interconnect extraction 1228 creates an R and C
http://www.google.com/patents/US6438729

Accelerate Design Closure. in-design, pre-LVS and post-extraction parasitic analysis. Handles large RC networks like power mesh; Interconnect calculator for
http://www.icscape.com/index.php/products/by-function/interconnect-analysis

IEEE Transactions on Very Large Scale Integration Inhee Lee, Qing Manycore Interconnect Fabric," IEEE Symposium on VLSI
http://blaauw.eecs.umich.edu/resource.php?grp=1

interconnect and substrate extraction software tool for techniques are used to accurately and efficiently extract these RC values from the layout.
http://www.optem.com/inspector.php

View Tony Nguyen's professional profile on LinkedIn. Strong background in custom IC Layout. Qing Zhu. Hoa Ngo. Sr. CAD Engineer at RFMD.
https://www.linkedin.com/pub/tony-nguyen/5/6B3/2B5

Inductance calculations, working formulas and extraction, substrate, VLSI interconnect. demonstrated by extraction from a real layout design that
http://citeseerx.ist.psu.edu/showciting?cid=211641

Calculating frequency-dependent inductance of VLSI interconnect by complete multiple reciprocity extraction. Several approaches a VLSI layout is considered
http://dl.acm.org/citation.cfm?id=1118299.1118491

by Qing K. Zhu, Zhu Qing K., Power Distribution Network Design for VLSI(1st Edition) by Qing K. Zhu, Interconnect RC and Layout Extraction for VLSI by
http://www.gettextbooks.com/author/Qing_Zhu

2007 IC/CAD Contest Problem B3 Interconnect Parasitic RC Extraction Source: Cadence Design Systems, Inc. 1. Introduction In submicron processes, signal delay due
http://www.ee.ncu.edu.tw/~cad_contest/Problems/95/PB3/2007_B3.pdf

by Qing Zhu, Wayne W.M. Dai, Joe G. Xi The clock network can exhibit distributed RC and lossy Our models comprehend key interconnect circuit and layout
http://citeseerx.ist.psu.edu/showciting?cid=935949
We focus on interconnect design, extraction, and 2D/3D substrate and interconnect RC extraction for detailed analysis of crosstalk and delay effects at the cell
http://s23.a2zinc.net/clients/MPAssociates/52DAC/Public/eBooth.aspx?FromPage=Exhibitors.aspx&ParentBoothID=&ListByBooth=true&BoothID=105458

Qing K. Zhu, "Interconnect RC and Layout Extraction for VLSI" Trafford Publishing | 2002 | ISBN: 155395369X | 150 pages | Djvu | 1,4 MB
http://avxsearch.se/?q=CADS%20RC

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http://www.amazon.ca/Interconnect-RC-Layout-Extraction-VLSI/dp/155395369X

interconnect RC is a significant portion of circuit performance, In a typical design flow, parasitic extraction and timing analysis are two independent steps.
http://doi.ieeecomputersociety.org/10.1109/VLSID.2006.148

Qing K. Zhu and Paige Kolze MOS Layout CHESS: A Comprehensive Tool for CDFG Extraction and Synthesis
http://www.computer.org/csdl/proceedings/isvlsi/2006/2533/00/01602405.pdf

Performance optimization of VLSI interconnect layout. Jason survey of existing techniques for interconnect optimization during the VLSI physical
http://www.sciencedirect.com/science/article/pii/S0167926096000089

High-Speed Clock Network Design has 2 available editions to buy at Alibris. " by Qing K. Zhu. Interconnect Rc and Layout Extraction for VLSI
http://www.alibris.com/High-Speed-Clock-Network-Design-Qing-K-Zhu/book/7622052
when compared to traditional layout extraction (2D PARASITIC EXTRACTION Interconnect capacitance in each node in a model for RC extraction, e.g, distributed
http://www2.computer.org/portal/web/csdl/doi/10.1109/SBCCI.2000.876050

The HDR Book: Unlocking the Pros Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits By Wenjian Yu, Interconnect RC and Layout
http://avxsearch.se/?q=RC%20BOOK
der Meijs, "Extracting Simple but Accurate RC Models for VLSI Interconnect. and layout extraction for interconnect resistance extraction by
http://citeseerx.ist.psu.edu/showciting?cid=2392566

State of the art in interconnect extraction is mostly RC. Post layout extraction for high frequency design On chip Interconnect Design of critical wires
http://www.research.ibm.com/haifa/Workshops/summerseminar2004/present/summer_phd_seminar04.pdf

and Y. Zheng, "Compression Algorithms for Dummy Fill VLSI Layout B. Yao and Z. Zhu K. Samadi and P. Sharma, "Interconnect Modeling for Improved
http://vlsicad.ucsd.edu/Publications/Conferences/

Extracting simple but accurate RC models for VLSI interconnect. From a background of RC interconnect models in layout-to and layout extraction for
http://citeseerx.ist.psu.edu/showciting?cid=842355

Optimization with Recourse of Analog Circuits including Layout Extraction, Capacitance of RC Interconnect, for VLSI Interconnect
http://users.ece.cmu.edu/~pileggi/publications/publications/

of the IFIP/IEEE International Conference on Very Large Scale Integration Q. Zhu, K . Vaidyanathan, O L. Pileggi, RC(L)Interconnect Sizing With Second
http://users.ece.cmu.edu/~pileggi/publications/refereed-conference-publications/

Postlayout EDA tools lock onto and a final performance simulation that uses interconnect RC Simon, "Technical White Paper on RC Extraction," Epic Design
http://www.edn.com/electronics-products/other/4348742/Postlayout-EDA-tools-lock-onto-full-chip-verificatio

In electronic design automation, parasitic extraction is calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an
http://en.wikipedia.org/wiki/Parasitic_extraction